# EGC220
# Class Notes
# 4/11/2023

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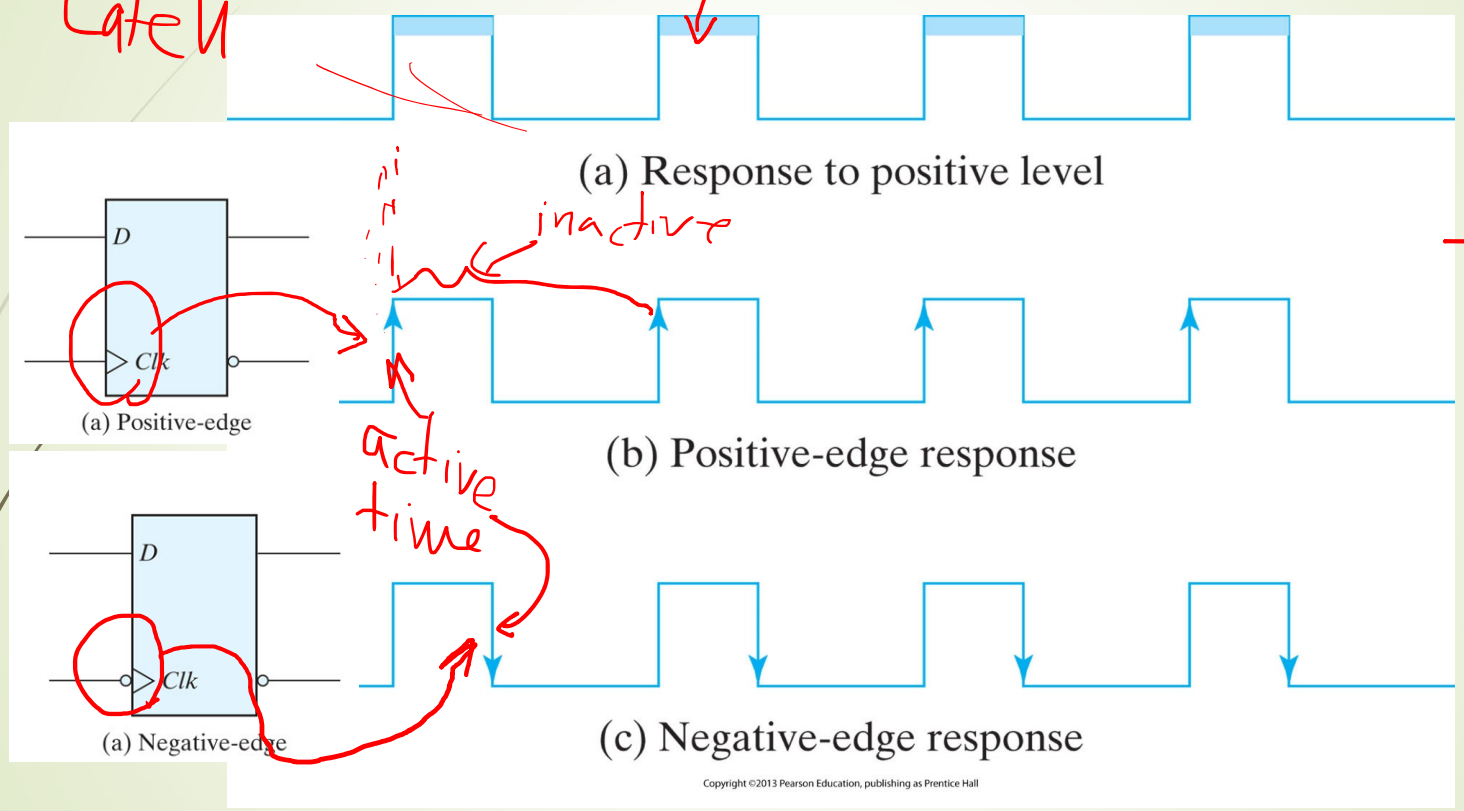
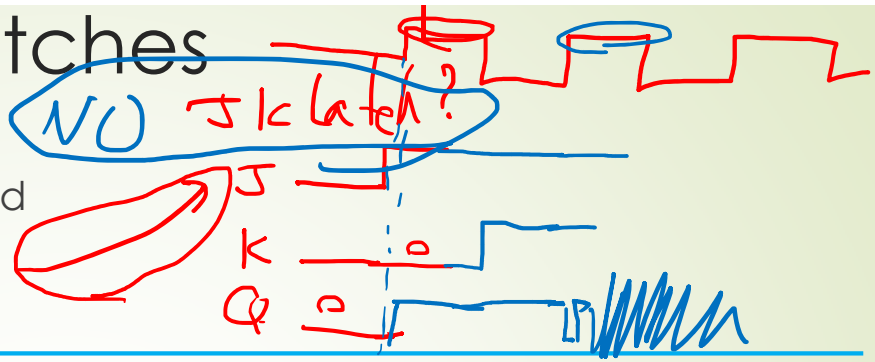
# Clock Response to Latch and Flip Flop




| D | Q(t+1) |
|---|---|
| 0 | 0 |
| 1 | 1 |

# Flip Flops Vs. Latches

- Flip flops are Edge Triggered
- Latches are level triggered

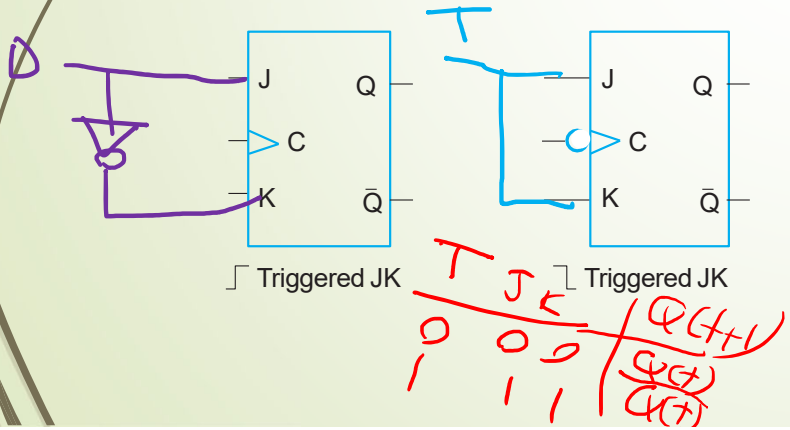


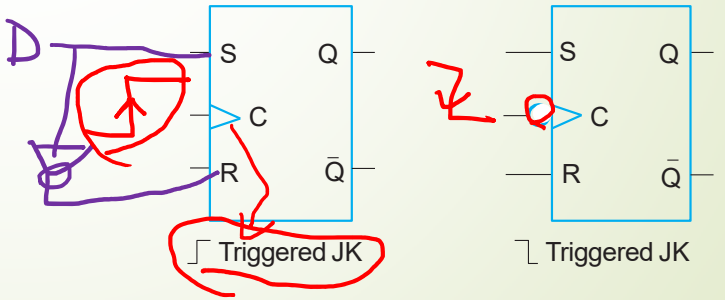
**(a) *JK* Flip-Flop**

| J | K | Q (t +1) | Operation |
|---|---|---|---|
| 0 | 0 | $Q(t)$ | No change |
| 0 | 1 | 0 | Reset |
| 1 | 0 | 1 | Set |
| 1 | 1 | $\overline{Q}(t)$ | Complement |

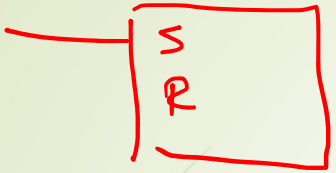
**(b) *SR* Flip-Flop**

| S | R | Q (t + 1) | Operation |
|---|---|---|---|
| 0 | 0 | $Q(t)$ | No change |
| 0 | 1 | 0 | Reset |
| 1 | 0 | 1 | Set |
| 1 | 1 | ? | Undefined |



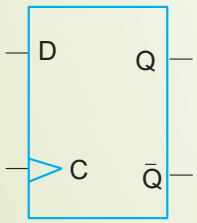



# Flip Flops Vs. Latches

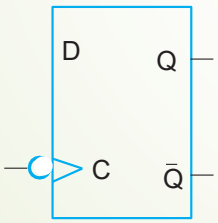



- Flip flops are Edge Triggered
- Latches are level triggered

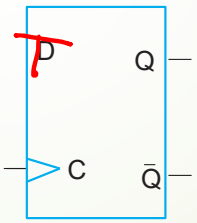
| (c) *D* Flip-Flop | | | (d) *T* Flip-Flop | | |
|---|---|---|---|---|---|
| **D** | ***Q* (*t* +1)** | **Operation** | **T** | ***Q* (*t* +1)** | **Operation** |
| 0 | 0 | Reset | 0 | $Q(t)$ | No change |
| 1 | 1 | Set | 1 | $\overline{Q}(t)$ | Complement |



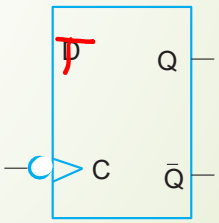
Triggered D



Triggered D

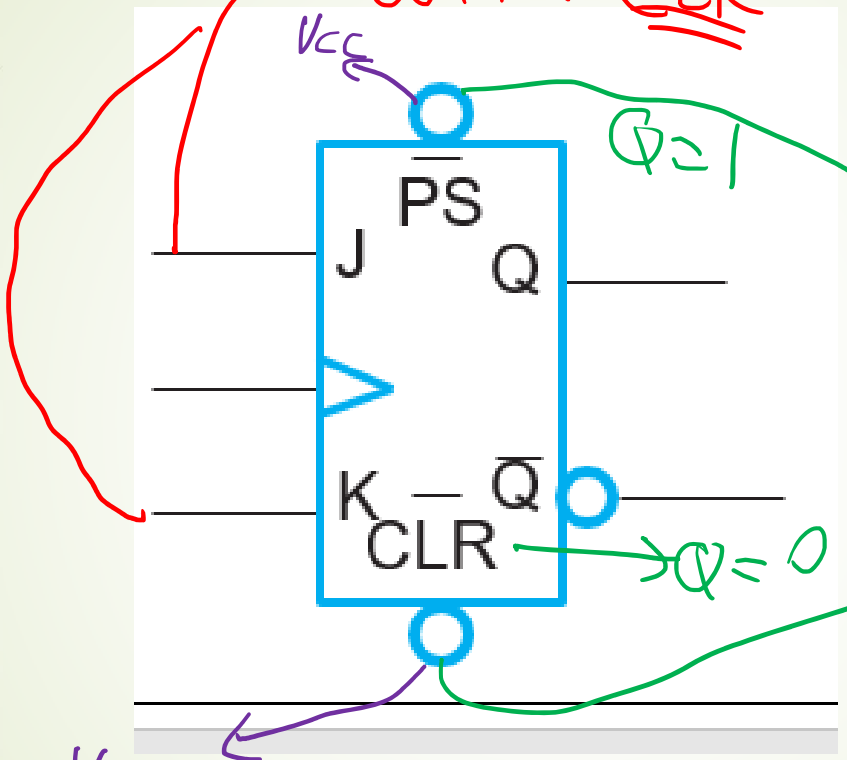


Triggered T



Triggered T

synchronous input: only active with CLK




characteristic table

Q=1

Asynchronous inputs independent of CLK

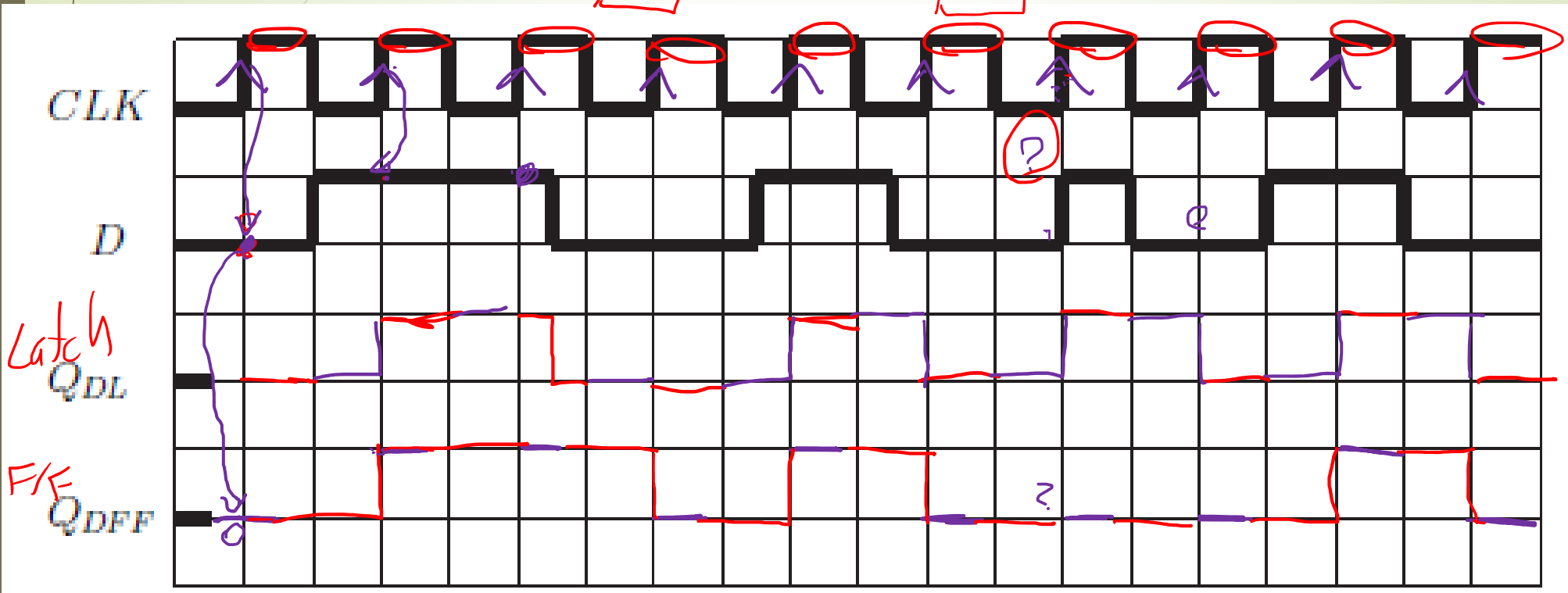
PS & CLR are low active

PS=0 ⇒ Q=1

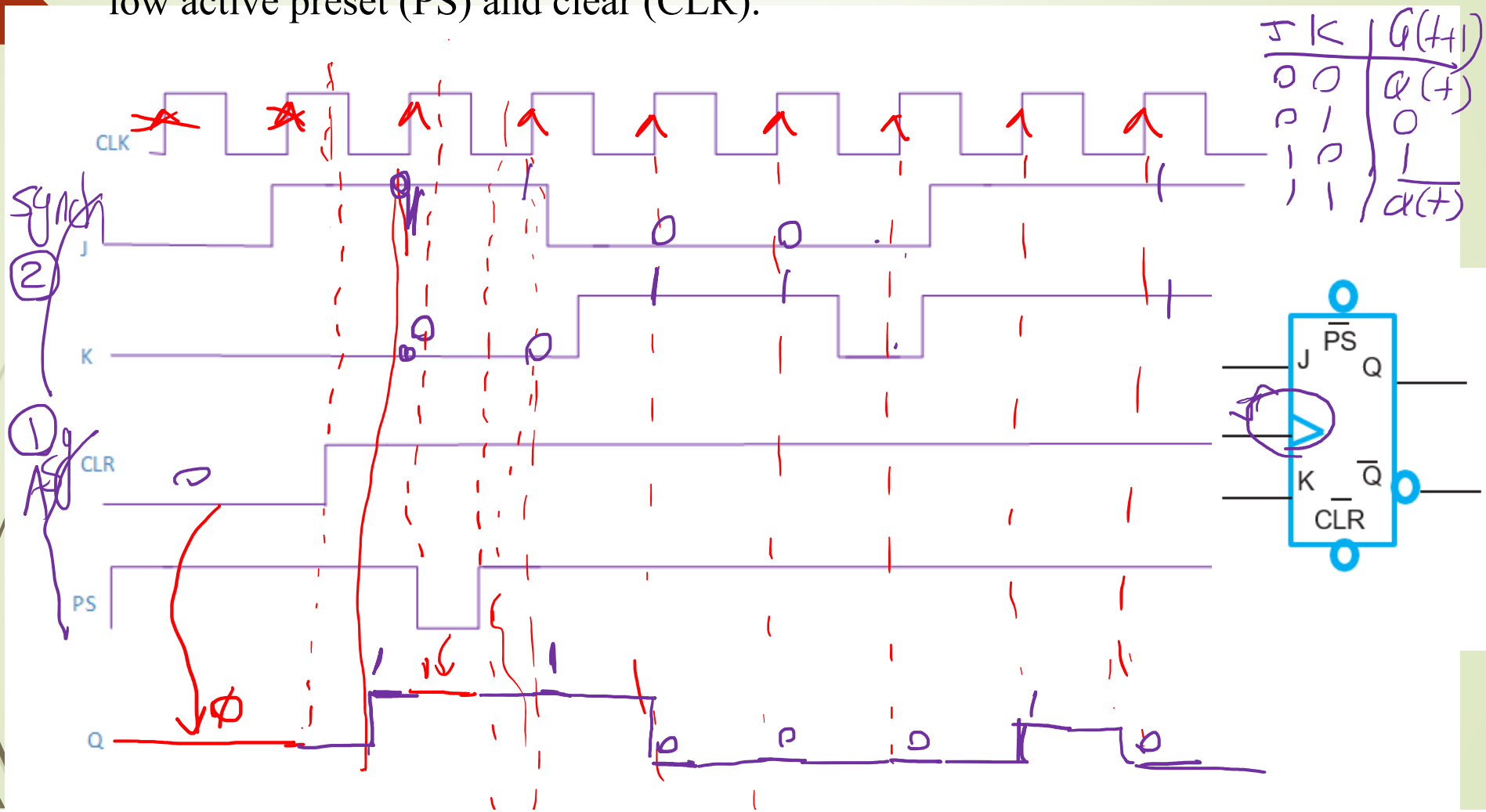
CLR=0 ⇒ Q=0

Problem 1

On the following graph, inputs CLK and $D$ are shown. They are inputs to both a D latch and a D flip-flop. CLK goes into the active high G input of the D latch and positive edge clock input of the D flip-flop. Show the output of the D latch as $Q_{DL}$ on the graph and the output of the D flip-flop as $Q_{DFF}$ on the graph. Both outputs are initially 0 at the start of the graph, as shown. Do the two outputs differ, and if so, why?



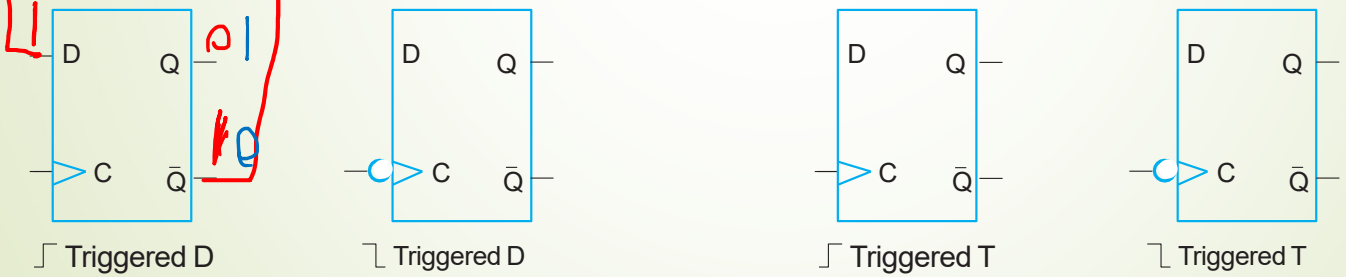
Problem 2. Complete the following timing diagram for a JK flip-flop with a low active preset (PS) and clear (CLR).

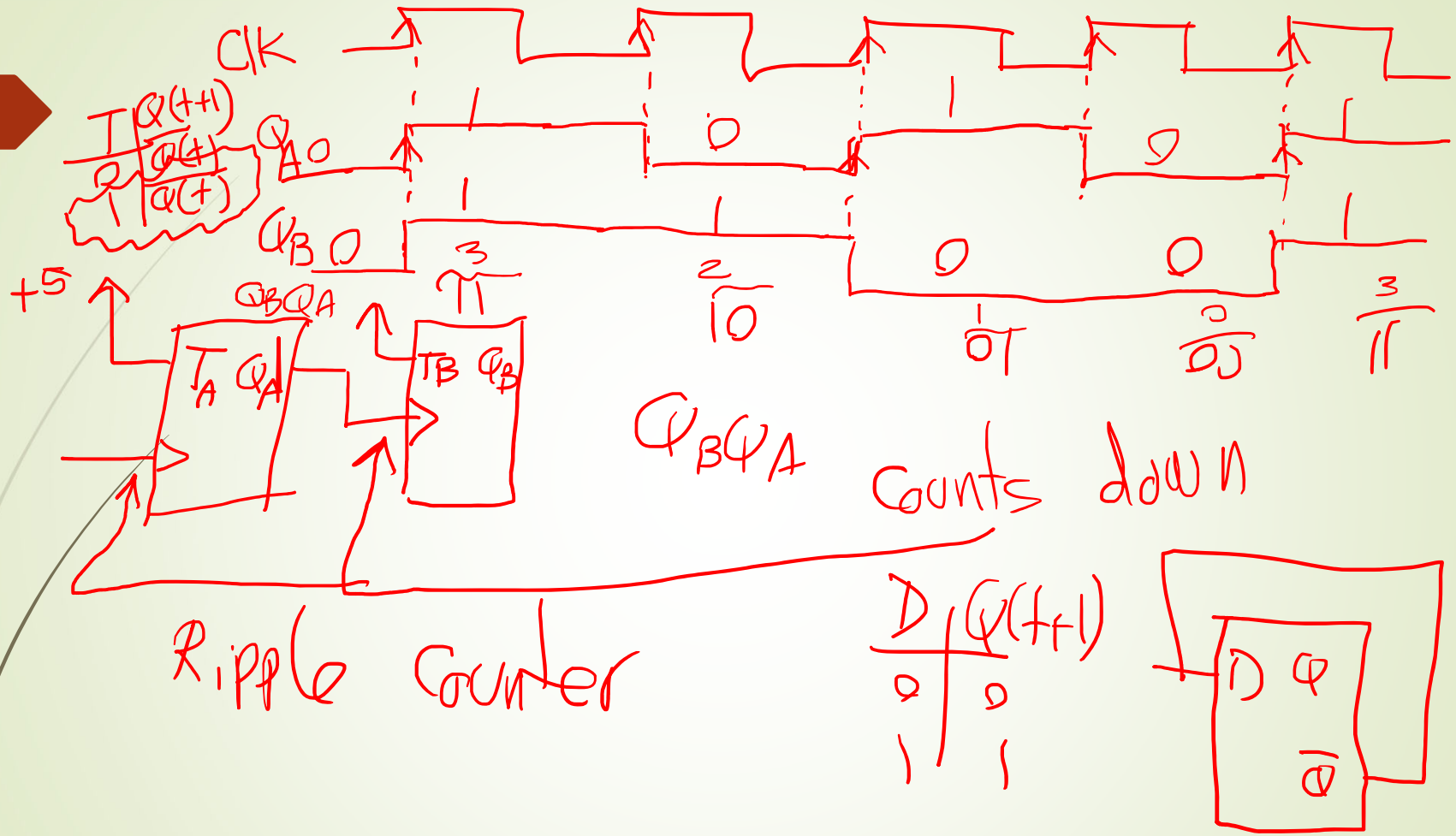


# Flip Flops Vs. Latches

- Flip flops are Edge Triggered
- Latches are level triggered

| (c) *D* Flip-Flop | | | (d) *T* Flip-Flop | | |
|---|---|---|---|---|---|
| **D** | ***Q* (*t* +1)** | **Operation** | **T** | ***Q* (*t* +1)** | **Operation** |
| 0 | 0 | Reset | 0 | $Q(t)$ | No change |
| 1 | 1 | Set | 1 | $\overline{Q(t)}$ | Complement |

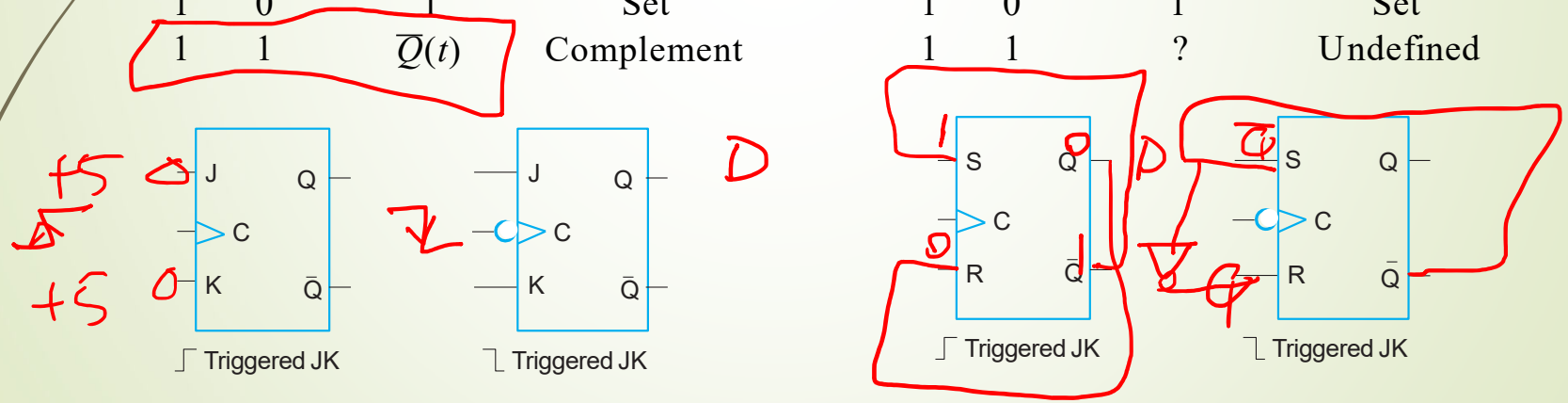



CLK
Q(t+1)
Q(t)
Q(t)
$Q_A$
$Q_B$
0
1
2
3
+5
$Q_BQ_A$
$T_A$ $Q_A$
$T_B$ $Q_B$
$Q_BQ_A$
Counts down
Ripple Counter
D
Q(t+1)
0
0
1
1
D
Q
$\overline{Q}$

# Flip Flops Vs. Latches

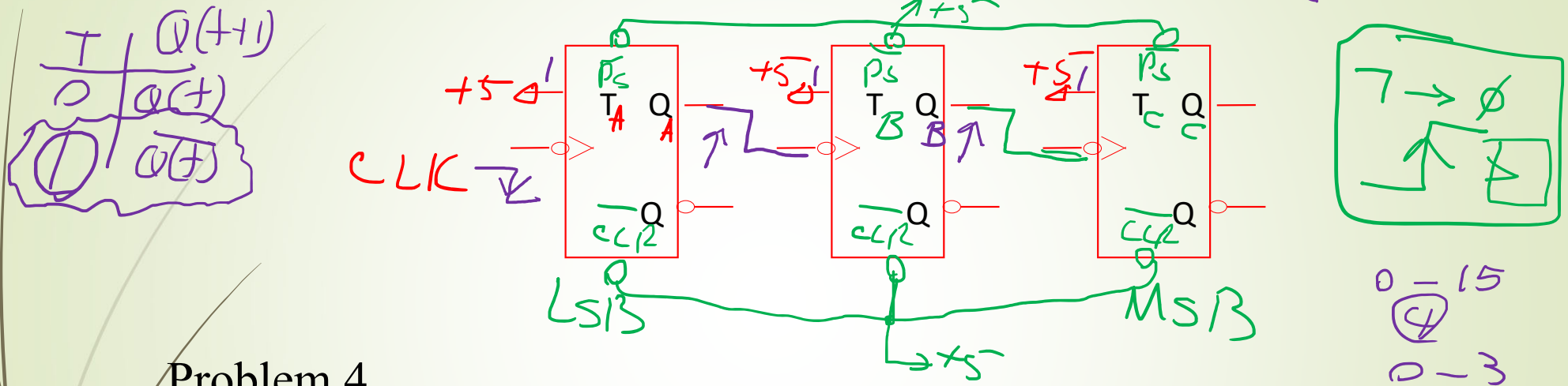
- Flip flops are Edge Triggered
- Latches are level triggered

| (a) *JK* Flip-Flop | | | | (b) *SR* Flip-Flop | | | |
|---|---|---|---|---|---|---|---|
| **J** | **K** | **Q (t +1)** | **Operation** | **S** | **R** | **Q (t + 1)** | **Operation** |
| 0 | 0 | $Q(t)$ | No change | 0 | 0 | $Q(t)$ | No change |
| 0 | 1 | 0 | Reset | 0 | 1 | 0 | Reset |
| 1 | 0 | 1 | Set | 1 | 0 | 1 | Set |
| 1 | 1 | $\overline{Q}(t)$ | Complement | 1 | 1 | ? | Undefined |



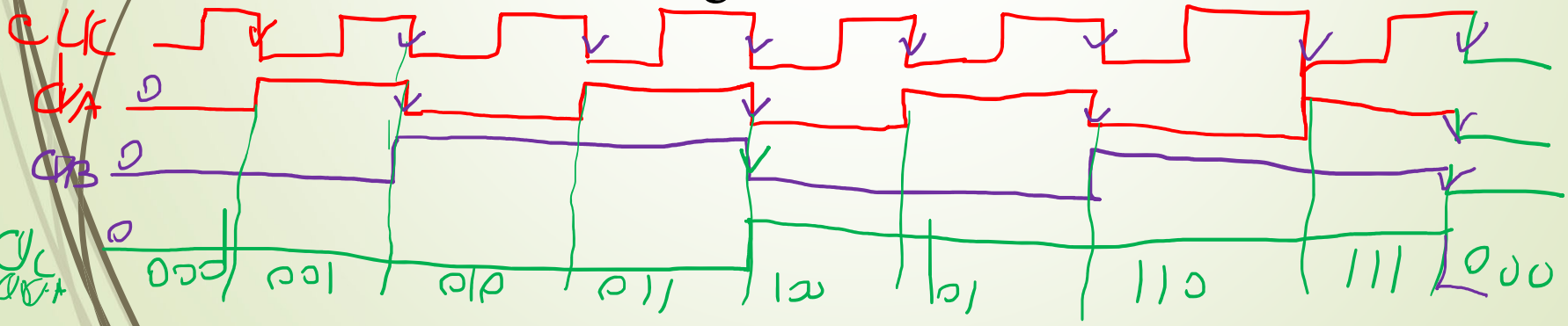
Problem 3

Using T flip-flops, design a ripple counter that counts 0 – 7 and repeats.



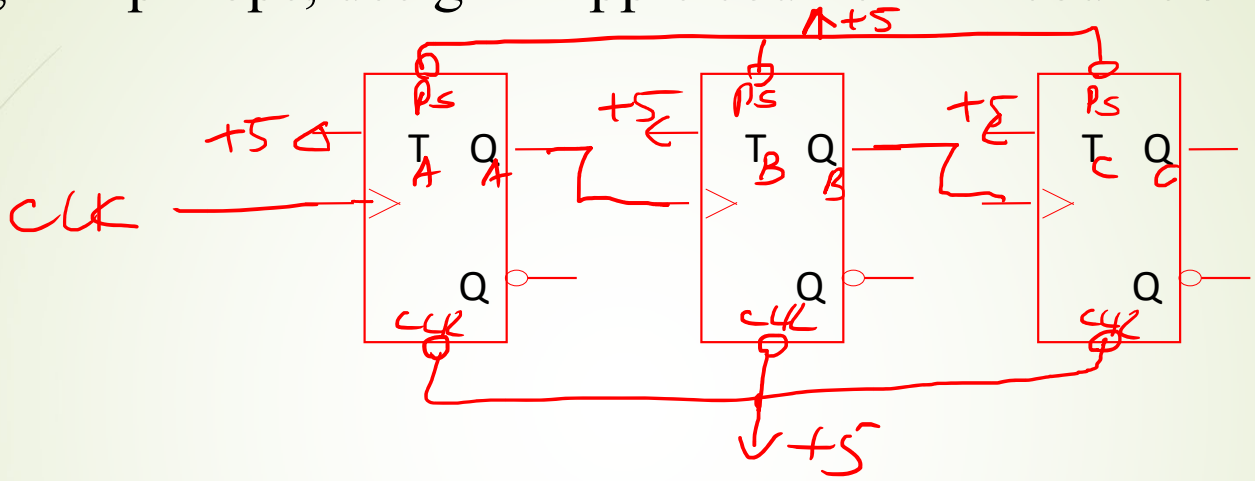

Problem 4

Show the waveform diagram for the counter in Problem 3.



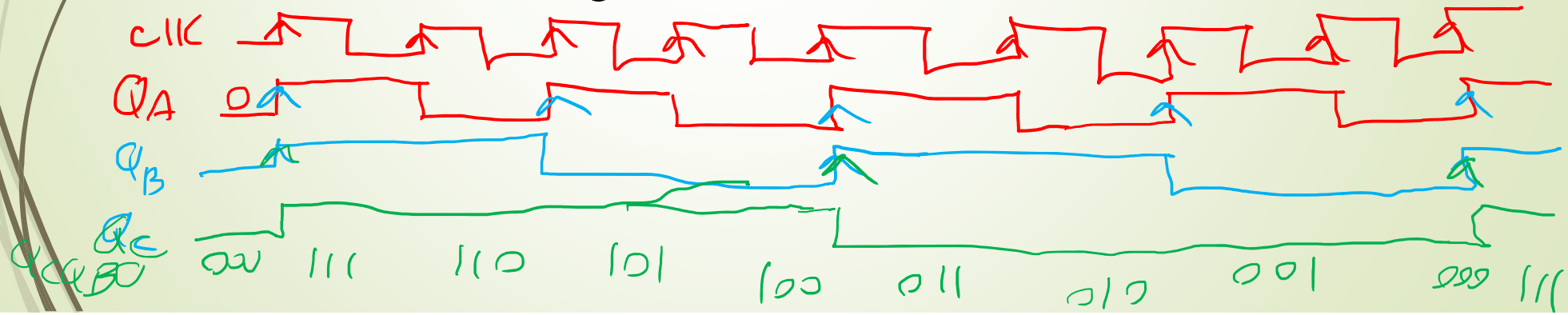
Problem

Using T flip-flops, design a ripple counter that counts 7 – 0 and repeats.



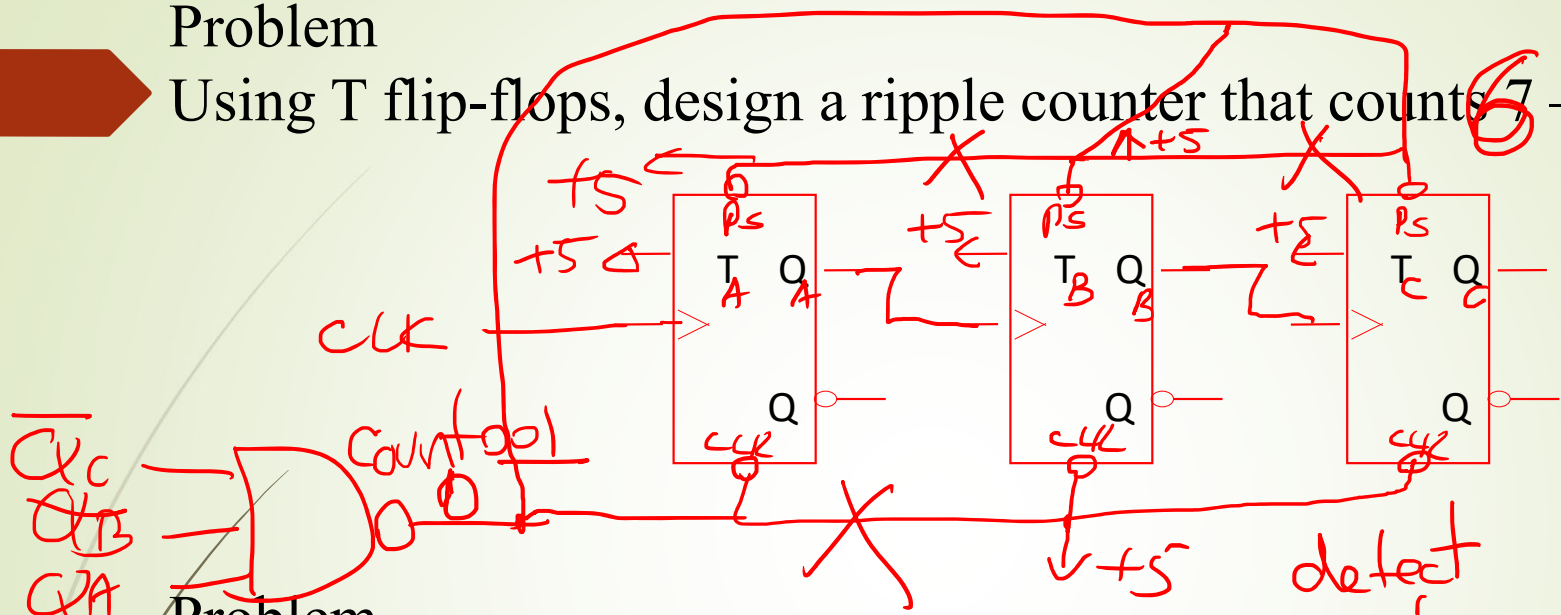

Problem

Show the waveform diagram for the counter in Problem .



Problem

Using T flip-flops, design a ripple counter that counts 7 – 2 and repeats.




Problem

Show the waveform diagram for the counter in Problem .